Pulse Power Amplifier Design
02/19/2011

Class A/B power amplifier design using MOSFET or GAN devices may utilize several circuit topologies to achieve pulse amplification with fast rise-time and minimal ringing. This paper will review several techniques with their attributes and limitation or short comings.

The most straight forward pulse amplifier design is to use Class A amplification for the driver stages to preserve pulse fidelity and operate the final output stages in Class B or AB to preserve DC to RF efficiency. The pulse modulation is derived from the exciter.

Pulse rise-time and fidelity is limited by the maximum stable rate of current change in the output stage without experiencing pulse ringing. Pulse ringing is caused by low frequency instability. Common source power amplifiers exhibit an increase in device gain a lower frequencies that can approach very high level with GAN and MOSFET device as they become voltage controlled current sources at low frequencies. The effect of increasing gain at low frequencies decreases the margin of stability when the device is not terminated with source and load resistances that will absorb any out of band reflections.

The need to faithfully amplify signals with wide baseband frequency content is very important in the design of any RF power amplifier. Pulse amplifiers fall into this category as they may have a constant carrier frequency but the pulse shape causes many sidebands to be generated. In order to reproduce the pulse faithfully the amplifier must be able to respond to the full bandwidth of the resulting signal. Broad band amplifiers with modern solid state devices have no problem in amplifying the power spectrum generated by such a RF pulse.

However, one must look closely at the average rate of current change in the amplifier. This is primarily in the output stage but can be also be a factor in the driver stage as well. It is the maximum rate of current change that determines the rise time rather than the static frequency bandwidth of the amplifier. If one takes a Class A stage, the average current stays the same whether the amplifier is idling or putting out full power. The response or rise time of a Class A amplifier is limited to its RF bandwidth as the instantaneous current is always available because of stored charge in the reactive matching circuitry and or the device itself. The energy expended in the peak RF cycle is recovered during the valley of the RF cycle. The device current remains the same.

In a non-linear power amplifier this is not the case. The current is a function of the power output. If the current cannot rise as fast as or faster than the input pulse or modulation envelope the full power output will be delayed by the amount of time it takes for the current to rise to the required value. The rate of current rise is primarily limited by the decoupling inductance in the drain

circuit. It is also limited by the availability of sufficient storage capacitance to supply the peak current.

In pulse amplifier design the challenge is to insure low source inductance and capacitive energy storage without terminating the amplifier with an unstable output load. The ideal impedance for the fastest rise time possible is a DC supply network that presents a device with high impedance at the RF center frequency and provides a short circuit at all frequencies below the carrier and modulation sidebands. Unfortunately if one accomplished this feat, the drain is effectively shorted at frequencies where the device is potentially unstable. This results in severe ringing or outright oscillation and perhaps even destruction of the part. It usually is a compromise to obtain the required rise time without excessive ringing or other instability. This is the primary limitation of obtainable rise time in other than class A RF power amplifiers.

It is important to fully understand these limitations before exploring alternate methods of pulse modulation.

It is possible to use a CW source at the carrier frequency and modulate the gate and or drain supplies.

Let's first look at just switching on and off the Vdd of the final stage with full gate RF drive applied. The first issue one would observe is the output of the PA would not drop to zero power during the pulse off time as semiconductor devices do not have very high RF isolation between gate and drain. A more subtle problem is that many RF devices will exhibit RF instabilities during operation at very low Vdd values. A third issue is the maximum RF gate voltage can be exceeded during periods of 0 Vdd. During normal operation the RF voltage swing on the gate is moderated by the internal capacitance of the device (Miller Effect). Once the device is turned off there is much less feedback to the gate and the RF voltage swing may increase to a level to cause catastrophic damage to the device.

Some of these effects can be mitigated by also switching off the driver stage. This is a very common practice as it avoids the possibility of gate or instability damage to the output device. It also improves the on to off ratio but generally will not prevent substantial leakage of RF during pulse off conditions. This technique is commonly used for AM modulation with envelope feedback to compensate for the non-linear function of the control voltage versus RF output power. The pulse rise time is very dependent on the rate the drain current can change. By switching the drain voltage the rise time of the power supply switch must be added to the overall rise time of the actual amplifier.

Polyfet experience with pulse amplifier is somewhat limited but we have seen instability when trying to pulse modulate with only controlling the drain voltage of the output device. It appears to be industry practice to modulate at least the driver and output stage to achieve a reasonable reduction in output power during modulation valleys or pulse off conditions. This technique is more commonly used for AM transmitters rather than for pulsed operation.

Another approach that has not been explored by Polyfet is to attempt turning off the gate by reducing the gate voltage to the point that the part does not draw current during the modulation peaks. There is a danger of voltage breakdown of the gate as it will take a very large negative voltage to overcome the RF drive peak voltage. One would have to apply this technique to the driver as well to yield a reliable design.

In summary Polyfet recommends caution in using voltage control of either the gate or drain of a signal device because of the risk of damage to the gate by overvoltage and or instability. Applying these techniques to multiple stages is a more robust and reliable approach. The cleanest technique although perhaps not the most efficient is to use a pulsed low level RF drive signal with fast rise times, design the driver for Class A operation to preserve pulse linearity and let the output stage be the limiting fact in achieving the fastest and the least amount of pulse ringing rise time.

This is not to say that switching the DC supply synchronous with perhaps the RF drive would achieve slightly improved results, but it will result in increased complexity of design.

In conclusion the design of the output device should include a method of decreasing the RF drive during the time the DC supply voltage is reduction to prevent device damage and instability.